

Hybrid 2D-3D Fast Electromagnetic Analysis aided by Pattern Recognition for Signal Integrity Analysis

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Abstract—The use of 3D full-wave electromagnetic solvers for signal integrity analysis is often hindered by its prohibitive time and memory requirements. In this work, a hybrid 2D-3D solver is proposed to address the computational challenges while still preserving the desired accuracy. The method is based on an image based segmentation technique followed by 2D-3D classification for each segment, analysis and cascading transfer functions. A figure of merit that accurately represents simulation accuracy in frequency domain is identified for the 2D-3D prescription. Numerical results for a 13” trace is presented and the benefit in simulation time versus accuracy are highlighted.

Keywords—Segmentation, network training, error metric, classification.

I. INTRODUCTION

Unlike the landscape of power, timing and noise aware design tools for silicon, the equivalent tools for package-board level design are not as efficient. This is primarily due to the requirement of 3D full-wave analysis at the system level [1] which presents a time and memory bottleneck. This inefficiency has restricted the use of tools to (a) prototyping small sections to provide electrical performance aware guidance on physical parameters at the design stage and (b) section-based modelling at the verification stage. The goal of this work is to enable full-system electrical characterization at a reduced time while still maintaining desirable accuracy. Current complexity of packages and boards used in SerDes applications and the associated bitrates require 3D full-wave EM analysis for accurate electrical characterization for several regions within the layout. However, there are regions within the layout that could be solved with a 2D assumption, where interconnects run for long lengths with a clean reference. The solver-on-demand technology has been introduced in the past to leverage this phenomenon. However, this requires manual intervention and expertise to classify sections for 3D or 2D analysis. Due to the massive complexity of co-existing vertical vias, horizontal interconnects and pads for passive components, it is extremely difficult to generalize an identification method of regions of the package-board layouts that could accurately be analyzed with a 2D assumption and those that require full 3D EM solution.

In this work, a methodology is proposed to segment the layout, automatically classify 2D or 3D usage for each segment followed by analysis and cascading of segment-based results for a full-system characterization. The images of the package-board layouts may be utilized for this purpose. A small study was conducted to understand if, like the fields of handwritten digit identification and facial recognition, there are underlying common features across segments of board layouts that could be used to extract principal

components or basis functions to represent the space of board layouts in general. Fig. 1 shows some training images of segments of boards with interconnects of different impedances and lengths for various high and low speed interfaces used to extract principal components for segments of boards.

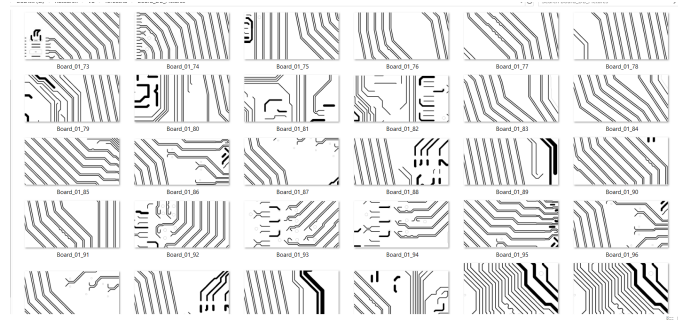


Fig. 1. Training set for PCB level routing images

These set of common features across boards with layouts of subsequent generation of SerDes designs can now be used to extrapolate electrical characteristics from past learnt images. In this work, the time-domain metrics like eye-height (EH) and eye-width (EW) are chosen as objective functions. The error between the 2D and 3D S-parameter results with respect to the desired objective is calculated using Feature Selective Validation (FSV) [2]. An Artificial Neural Network (ANN) is trained on segmented PCB images to output the FSV value which is then utilized to classify the segments as 2D or 3D. The various solver runs on segments is then performed and the S-parameters of the segments are finally cascaded to give the end to end S-parameters of the entire channel.

The paper is organized as follows: section II describes the image segmentation method and challenges. In section III the error metric FSV is discussed. In section IV the ANN based approach to predict the error metric is presented. The numerical results for a single 13” interconnect segmented and cascaded is shown in section V.

II. INTERCONNECT ISOLATION & IMAGE SEGMENTATION

The first step of the methodology is to isolate high-speed SerDes interconnects or buses from a complex package-board layout and segment them into smaller regions as shown in Fig. 2. The isolation of interconnects of a specific interface is done using the bw-boundaries [3] function implemented in MATLAB. The image of a specific layer of the package/board must be first converted to a binary image to use this algorithm. Once a trace is isolated, it is segmented using Simple Linear Iterative Clustering (SLIC) [4], an algorithm that forms super-pixels or segments based on similarity in color and proximity in space for each pixel in the image.

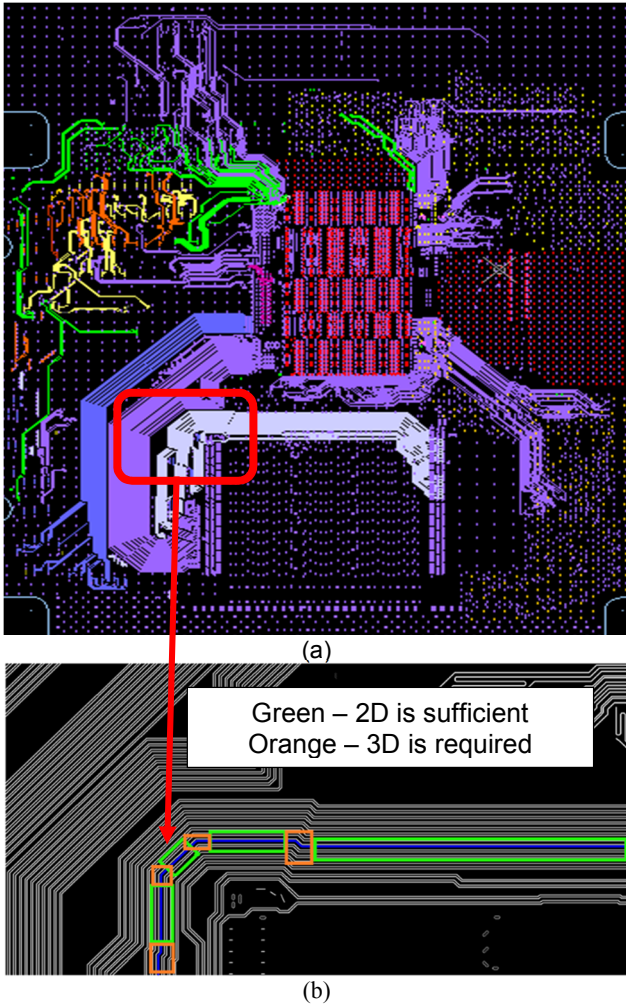


Fig. 2. (a) Top layer of complex PCB (b) Image segments

For example, a 13", 50 ohm impedance micro-strip trace made of PEC in vacuum, with a geometry as shown in Fig. 3 is used. After running the bw-boundaries and SLIC algorithms on this trace, the super-pixels or segments formed are as shown in Fig. 3 in pink and red respectively.

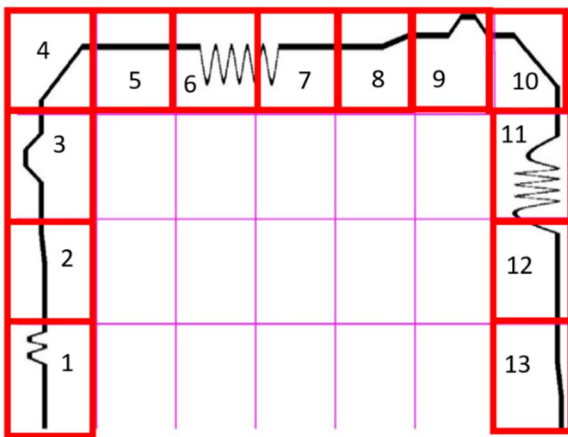


Fig. 3. Bw-boundaries and SLIC on an interconnect image

As can be seen from Fig. 3, SLIC has some limitations with regards to the segmentation done between segments 6-7 and 11-12. Other geometry based segmentation methods that utilize the generation and location of "nodes" in the odb++ format are being studied in parallel to overcome the limitations of SLIC for segmentation in this methodology.

III. ERROR METRICS FOR CLASSIFICATION

An error-metric needs to be defined for classification of segments for 2D or 3D analysis. For signal integrity applications the error in EH and EW seen at the receiver port of an interconnect segment using full-wave 3D extraction can be compared against that using 2D. Norm-by-norm error ϵ_N , as defined in (1) is a well-known metric to measure difference between two sets of S-parameters.

$$\epsilon_N = \frac{\text{norm}(S_{3D} - S_{2D})}{\text{norm}(S_{3D})} \quad (1)$$

However, it has the tendency to amplify a slight difference between two curves showing minimal shift in resonance to a relatively large error number. The FSV method is proved to do this well and details about the method and its implementation can be found in [2]. In this section the effectiveness of FSV as compared to norm-by-norm for 2D/3D classification is studied.

In the example shown here, a segment of interconnect is solved in both full-wave 3D and 2D solvers and s-parameters are extracted. The error between these s-parameters is calculated using norm-by-norm and FSV methods. The error-metrics are then correlated to the delta change in EH and EW for segments with increasing electrical lengths from $\lambda/2$ to λ at 10GHz. The correlation matrix is shown in Table 1.

TABLE I: CORRELATION MATRIX FOR ERROR METRICS

	EYE_H	EYE_W	FSV	NORM 2
EYE_H	1	.8935	.8499	.5456
EYE_W	.8935	1	.6607	.2352
FSV	.8499	.6607	1	.7702
NORM 2	.5456	.2352	.7702	1

For demonstration purpose a test is performed with varying angular bend in the interconnect segment as shown as inset of Fig. 4. As expected, with increase in the bend angle the error between the 3D and 2D results increase as shown in Fig. 4b.

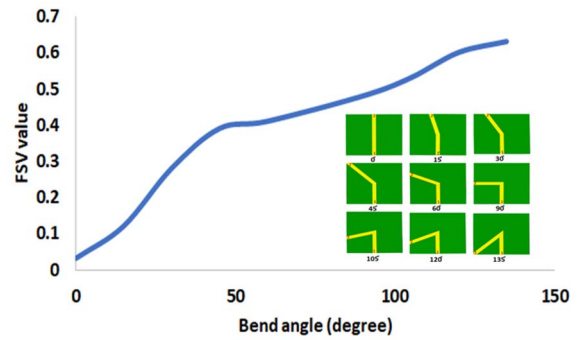


Fig. 4. FSV values for varying bend angles

IV. PCA, ANN & SEGMENT CLASSIFICATION

The segments of the PCB at high resolution are both redundant and expensive for any machine learning algorithm that would use it as input. Hence some form of dimensionality reduction is required to store and process the images of segments. For this work, Principal Component Analysis (PCA) was chosen as the dimensionality reduction operator. The coefficients of the principal components are then used as inputs to a multi-layered perceptron (MLP). The MLP is trained to predict the error between the 3D and 2D solved S-parameters of the interconnect/s in the board segment as

shown in Fig. 5a. For this paper, the first 300 principal components of the 625 (25 x 25) pixels of the image were taken as input to an ANN [5] with one hidden layer of 30 neurons mapping to one output. The ANN was configured as a feed-forward net with the constants tuned over several iterations to give minimum training and validation error. The training set was randomly distributed as 70% training and 30% validation data. The prediction of S-parameters' error over the validation set is shown in Fig. 5b.

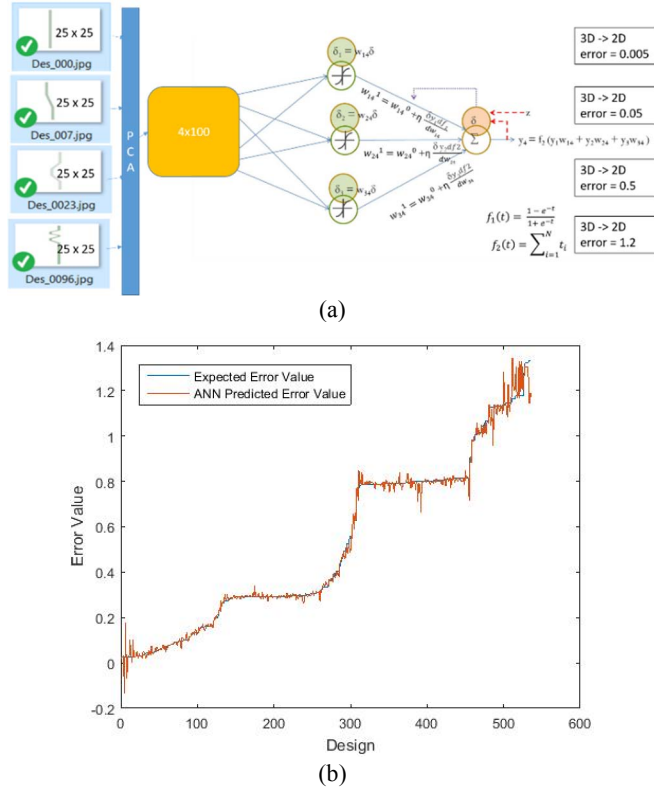


Fig. 5 (a) Block diagram showing inputs and outputs of the classification system (b) Predicted error over validation set

V. NUMERICAL RESULTS

A PCB interconnect with the layout and stack-up as shown in Fig. 6, is used as a test case for the methodology presented. A segmentation process as described in section II was performed on the interconnect, yielding six segments as shown in red boxes in Fig. 7.

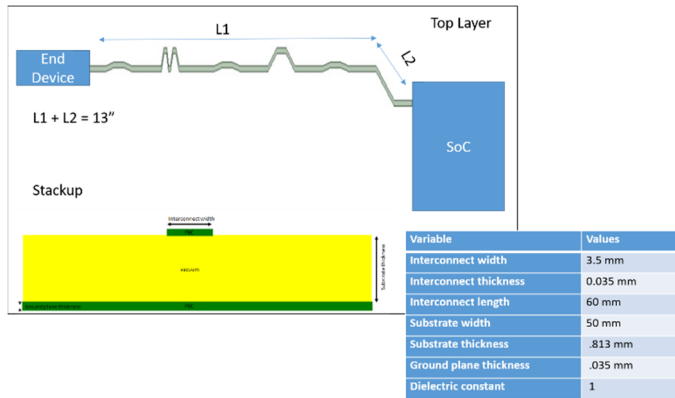


Fig. 6. Interconnect Stack-Up and Geometry

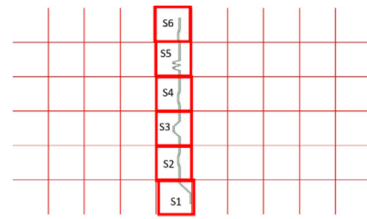


Fig. 7. SLIC segments on the interconnect of Fig. 9.

The trained ANN predicted the error metric of the six segments with 93.05% accuracy with a maximum error of 0.0265. Based on the error spread across the training cases, the threshold for 2D-3D classification was set to 0.2, leading to segments S1,2,4,6 of Fig. 7 being classified as '2D solve ok'. The loss in accuracy is minimal across the full 3d solve as compared to the cascaded solve as seen from Fig. 8. The time taken to solve the system using several combinations described in Table II.

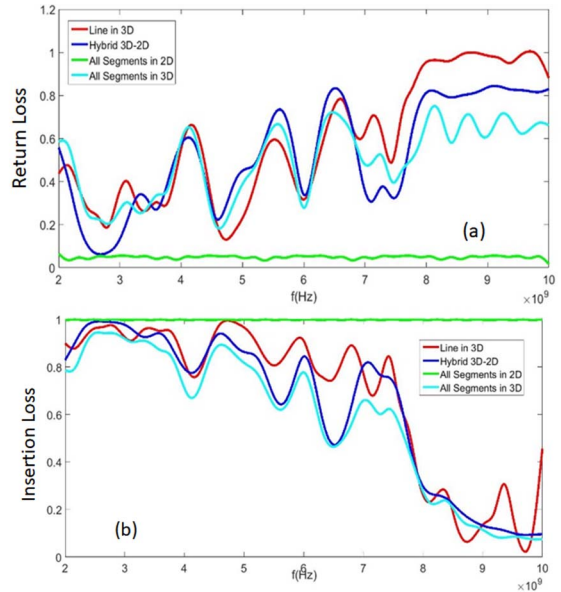


Fig. 8. (a) Return Loss (RL) (b) Insertion Loss (IL) for different cascading combinations

TABLE II: SOLVE TIME COMPARISON

Method	Full-wave 3D	Hybrid 3D-2D	All 3D Segments	All 2D Segments
Time (Min)	108	44	66	~0
* Each segment takes 11 min to solve in full-wave 3D				
* Time to solve in 2D is extremely small and ignored for this work				
* Cascading overhead is extremely small and ignored for this work				

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